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| Examiner<br>Initials* | Cite<br>No. <sup>1</sup>  | Foreign Patent Document |        |                    | Name of Patentee or<br>Applicant of Cited<br>Document | Date of Publication of Cited Document<br>MM-DD-YYYY | T |
|-----------------------|---|-------------------------|--------|--------------------|---|---|---|
|                       |   | Office <sup>2</sup>     | Number | Class/<br>Subclass |   |   |   |
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| Examiner<br>Signature |  |                         |        |                    | Date<br>Considered                                    | 6/25/04   |   |

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| Substitute for form 1449A/PTO                            |   |    |   | <b>Complete if Known</b> |                      |
|  |   |    |   | Application Number       | Unassigned           |
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b> |   |    |   | Filing Date              | Filed Herewith       |
|  |   |    |   | First Named Inventor     | Richard A. Blanchard |
| (use as many sheets as necessary)                        |   |    |   | Group Art Unit           | 2811                 |
|  |   |    |   | Examiner Name            | Unassigned           |
| Sheet  | 2 | of | 2 | Attorney Docket Number   | GS 124 D1            |

| <b>OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS</b> |                          |   |                |
|--|--------------------------|---|----------------|
| Examiner<br>Initials*                                    | Cite<br>No. <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T <sup>2</sup> |
| TJN  | 1                        | Baliga, B. Jayant, Chapter 7, "Power Mosfet: 7.1 Basic Structure and Operation," PWS Publishing (Boston, 1996), pp. 336-339.  |                |
|  | 2                        | Wolf, Stanley et al., "Silicon Processing for the VLSI Era", Vol. 1: Process Technology," Lattice Press, Sunset Beach, CA, (1986), pp. 321-323.   |                |
|  | 3                        | Wilson, Syd R., et al., "Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey, (1993), pp. 42-59; 867-872.  |                |
|  | 4                        | IBM Technical Disclosure Bulletin, "Fabrication of Narrow Self Aligned Trenches and Isolated N-Type Silicon Region With buried N+ Layer," Vol. 34, No. 10A, (March, 1992), pp. 397-399.   |                |
|  | 5                        | Gary E. McGuire, "Semiconductor Materials and Process Technology Handbook," Noyes Publ., Norwich, New York, (1988), p.18.   |                |
|  | 6                        | Hu, Chenning, "Optimum Doping Profile for Minimum Ohmic Resistance and High-Breakdown Voltage," IEEE Transactions on Electron Devices, Vol. ED-26, No. 3, March 1979, pp. 243-244.  |                |
| TJN  | 7                        | Grove, A. S., Physics and Technology of Semiconductor Devices, 3.7, "The Redistribution of Impurities in Epitaxial Growth," pp. 78-83, John Wiley and Sons, Inc. New York, 1967.  |                |
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| Examiner<br>Signature |  | Date<br>Considered | 6/22/04 |
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